#13/D
TBC
3-703

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Hieu Van TRAN et al.

Serial No.: 09/929,542 Group Art Unit: 2824

Filed: August 13, 2001 Examiner: Dinh, Son T.

Title: **ARRAY ARCHITECTURE AND OPERATING METHODS FOR DIGITAL MULTILEVEL NONVOLATILE MEMORY INTEGRATED CIRCUIT SYSTEM**

Certificate of Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as FIRST CLASS MAIL in an envelope addressed to: **BOX RCE**, Commissioner of Patents, Washington, D.C. 20231, on:

February 25, 2003

Rosa A. Caviedes

Rosa A. Caviedes

* * *

AMENDMENT

Box RCE
Commissioner for Patents
Washington, DC. 20231

Sir:

In response to the Office Action mailed on August 27, 2002, please cancel claim 83 without prejudice, and please amend claim 4 as follows: (marked up version of claim in Appendix)

---

4. (twice amended) A data storage system comprising:

a plurality of multidimensional segmented memory arrays, each memory array including a plurality of memory cells, a plurality of bit lines, a plurality of control gate lines, and at least one common line, wherein each memory cell is configurable to store one of 2^N values where N is two or greater;

at least one memory decoder coupled to the memory arrays, each memory decoder configured to provide bias signals to selected ones of the plurality of memory cells; and